REMARKS/ARGUMENTS

In the Office action dated February 17, 2004, the Examiner raised several objections to the specification and the claims and rejected claims 1 - 20 under 35 U.S.C. § 103.

The above identified patent application has been amended and reconsideration and reexamination are hereby requested. Applicant has amended the specification to correct typographical errors. Applicant also has amended claims 1, 7 - 9 and 19. Claims 1 - 20 remain pending in the application.

Applicant's Amendments the Claims

Applicant has amended claims 1, 7 and 19 to correct several typographical errors. Applicant submits that these amendments do not narrow the scope of the claims.

Applicant's Response to the Objections to the Specification

Applicant has amended the specification as set forth above to correct the typographical errors identified by the Examiner and other typographical errors. Applicant submits that no new matter is added by this Amendment as the intended text (as corrected) is evident from the text as originally submitted.

Applicant's Response to the Objections to the Claims

Applicant has amended claims 7, 8 and 9 as suggested by the Examiner.

Response to the Rejection of the Claims Under 35 U.S.C. § 103

The Examiner rejected claims 1 - 20 under 35 U.S.C. § 103(a) as being unpatentable over Hobson et al. (U.S. Patent No. 6,209,016). Claims 2 - 20 are dependent on independent claim 1.

Applicant respectfully submits that claim 1 is not obvious in view of Hobson et al. because Hobson et al. does not teach or suggest an "execution unit including at least one adder and at least two multipliers" in combination with a "decode unit configured to determine if a square operation or a product operation needs to be performed on an operand, the decode unit further configured to issue instructions so that certain multiply and/or addition operations are performed in parallel in the execution unit while performing either the square or product operation."

At paragraph 4.2 of the Office action the Examiner states that these limitations are taught by Hobson et al. in Figures 3 and 4, column 6, lines 44 - 49 and column 4, lines 27 - 40 and claim 7 and that it would have been obvious to modify Hobson et al. to configure the decode unit to issue instructions so that multiplication and addition operations are performed in parallel in the execution unit while performing either the square of product operation.

Applicant respectfully disagrees. The portion of column 6 in Hobson et al. cited by the Examiner refers to the prior art co-processor of Figure 1. Here, the CPU examines the "current bit to decide whether to perform a modular square of a modular multiply." Thus, Hobson et al. does not teach the claimed combination in an encryption processor of "a decode unit,

coupled to the execution unit, the decode unit configured to determine if a square operation or a product operation needs to be performed on an operand."

Moreover, the portion of column 4 in Hobson et al. cited by the Examiner teaches splitting a serial bit stream "into two (odd and even) component bit streams (bits from the originating serial bit stream are fed alternately into the two component bit streams respectively) and the two component bit streams are processed in parallel, one bit being presented by each of the component bit streams at the same time to form a bit-pair for calculation." Thus, all addition, subtraction and multiplication operations are performed in parallel on alternating bits of data from a serial data stream. Consequently, Hobson et al. does not teach or suggest selectively performing operations in parallel. Moreover, Hobson et al. does not teach or suggest selectively performing square or product operations in parallel.

In contrast, the invention of claim 1 provides an efficient method of performing an operation on an operand by selectively performing square or product operations in parallel. This is set specifically forth in claim 1 which claims a decode unit "configured to issue instructions so that certain multiply and/or addition operations are performed in parallel in the execution unit while performing either the square or product operation." Accordingly Applicant submits that the invention of claim 1 is not obvious in view of Hobson et al.

Claims 2 - 20 that depend on claim 1 also are patentable over the cited references for the reasons set forth above. In

addition, these dependent claims are patentable over these references for the additional limitations that the dependent claims contain.

SUMMARY

In view of the above amendment and remarks it is submitted that the claims are patentably distinct over the cited references and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Respectfully submitted,
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